



**Ahsanullah University of Science and Technology**  
**Department of Electrical and Electronic Engineering**

LABORATORY MANUAL  
FOR  
**ELECTRICAL AND ELECTRONIC SESSIONAL COURSES**

**Student Name :**

**Student ID :**

**Course No. : EEE 4138**

**Course Title : Digital Electronics II Lab**

**For the students of**  
**Department of Electrical and Electronic Engineering**  
**4th Year, 1st Semester**

## EXPERIMENT # 1: DIODE-RESISTOR LOGIC (DRL)

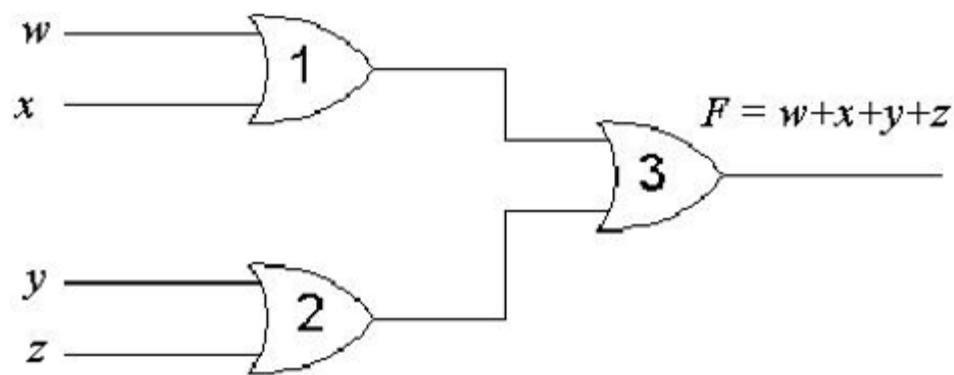
### OBJECTIVES:

- I. To study the AND & OR gates Constructed by using the Diode Logic (DL).
- II. To construct a wired-logic OR gate and verify its operation.

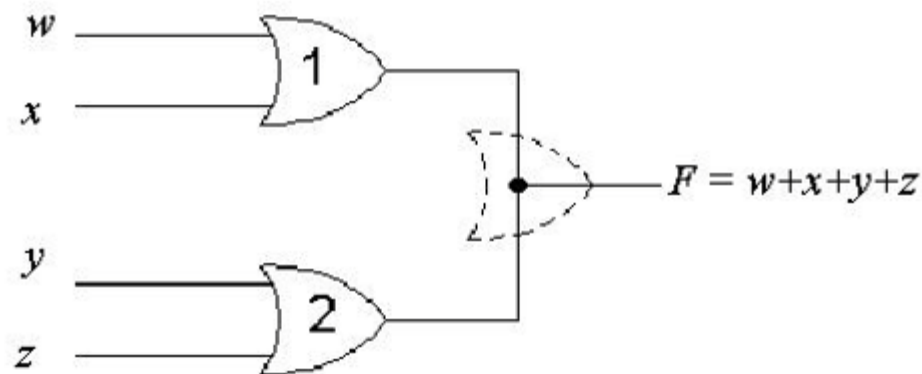
**EQUIPMENTS:** Power supply, digital multimeter, diodes (1N4007) and resistors.

### BACKGROUND:

In the first part of this experiment positive-logic AND, OR gates will be constructed using diode logic. That is, logic 0 state will be requested as LOW, while logic 1 state will correspond to HIGH.



(a)



(b)

Figure 1 : Wired-Logic OR gate .

To explain the concept of wired-logic, consider the Boolean function  $F(w,x,y,z) = w+x+y+z$ , implemented by two-input OR gates as shown in Figure 1 (a). Considering that each OR gate is constructed by using diode logic, as in part I of this experiment, it can be shown that the OR gate 3 is redundant, and the outputs of OR gates 1 and 2 can be directly wired together, as shown in Figure 1 (b), without affecting the implementation of the above function  $F$ . This is known as wired-logic.

**PROCEDURE:**

**PART I: Positive-Logic AND Gate:**

1. Construct the circuit as show in Figure 2.

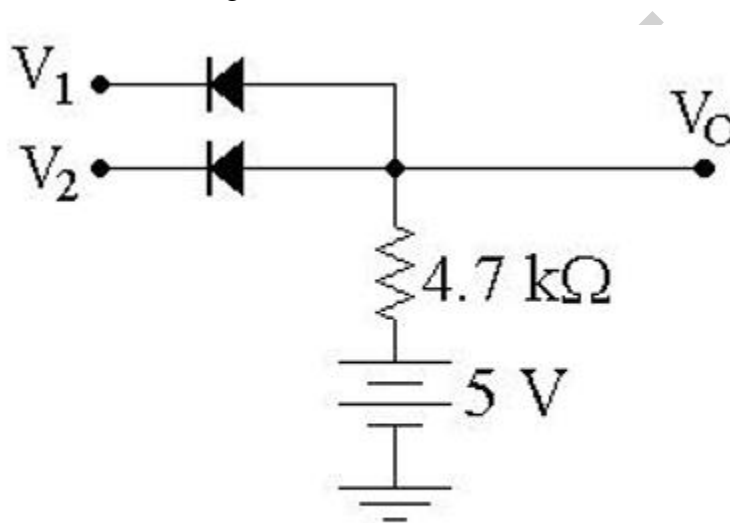


Figure 2 : Positive Logic AND Gate.

2. Measure the output voltage  $V_O$  for the four different combinations of input voltages  $V_1$  and  $V_2$  as given in Table I.

Table I: Input/Output voltages for the DL AND gate

$V_1$ (Volts)	$V_2$ (Volts)	$V_O$ (Volts)
0	0	
0	5	
5	0	
5	5	

**Positive-Logic OR Gate:**

1. Construct the circuit as show in Figure 3.

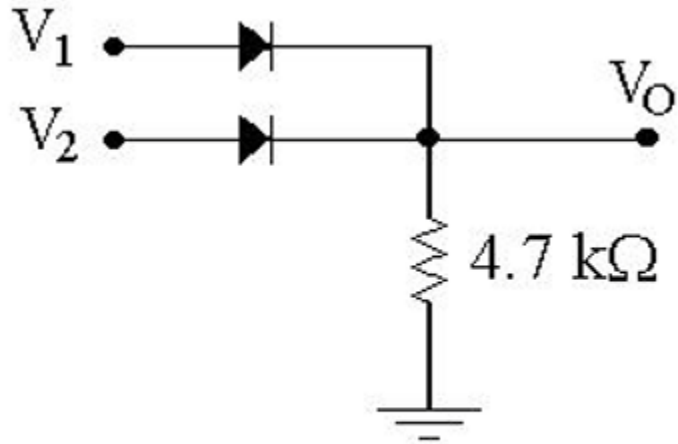


Figure 3 : Positive Logic OR Gate.

2. Measure the output voltage  $V_O$  for the four different combinations of input voltages  $V_1$  and  $V_2$  as given in Table II.

Table II: Input/Output voltages for the DL OR gate.

$V_1$ (Volts)	$V_2$ (Volts)	$V_O$ (Volts)
0	0	
0	5	
5	0	
5	5	

## PART II:

### Wired Logic

1. Construct the circuit as show in Figure 4.

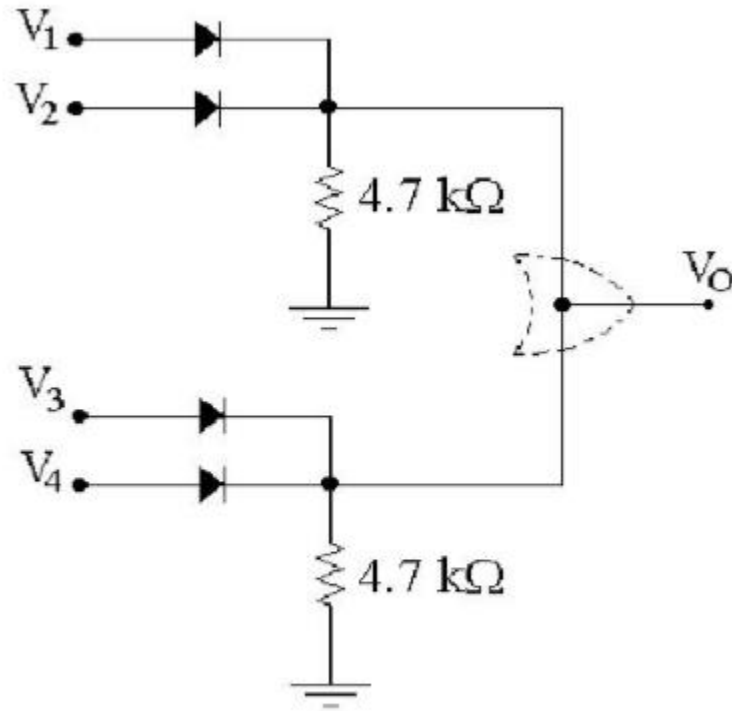


Figure 4 : Wired- Logic OR Gate.

2. Measure the output voltage  $V_O$  for different values input voltages and fill Table III with the measured values.

Table III: Wired-Logic OR gate

$V_1$ (Volts)	$V_2$ (Volts)	$V_3$ (Volts)	$V_4$ (Volts)	$V_O$ (Volts)
0	0	0	0	
0	0	0	5	
0	0	5	0	
0	5	0	0	
5	0	0	0	
5	0	5	0	
5	5	5	5	

### DISCUSSION:

1. On the basis of your results obtained in Table I, show that the circuit of Figure 2 behaves as AND gate for positive logic, but it will function as an OR gate for negative logic. Similarly, show that the results of Table II indicate the circuit of Figure 3 behaves as an OR gate for positive logic and as an AND for negative logic.

2. Explain why the measured values of output voltage in Table I and II are different from those obtained by using “ideal” diodes. 3- Using your results in Table I and II, calculate the power dissipation in the AND & OR gates implemented in circuits of Figure 2 and 3, respectively. Explain your procedure.

**PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Verify theoretically that circuit of Figure 4 is in fact a 4-input OR gate.
2. Draw a wired-logic AND gate to implement the function:  $F(w, x, y, z) = w.x.y.z$

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## EXPERIMENT # 2: THE BJT INVERTER (RTL)

### OBJECTIVES:

- (i) To draw the transfer characteristics of the BJT inverter and to determine its noise margins.
- (ii) To observe and to determine (approximately) the propagation delay times.

**EQUIPMENT:** Power supply, function generator, oscilloscope, digital multimeter, potentiometer, resistors and BJT transistor.

### BACKGROUND:

A BJT inverter is a simple CE switch as shown in Figure 1 (a). When the input voltage  $V_i$  is LOW, the output voltage  $V_o$  is HIGH and vice-versa. Its voltage transfer characteristics are such as shown in Figure 1 (b). The noise margins  $NM$  can be determined from the transfer characteristics as follows:

$$NM_H = V_{OH} - V_{IH}, \text{ (Volts)}$$

$$NM_L = V_{IL} - V_{OL}, \text{ (Volts)}$$

The higher noise margins, the higher are the immunity of the logic gate to unwanted signals (noise). A noise of amplitude less than  $NM$  will not alter the logic state of the gate.

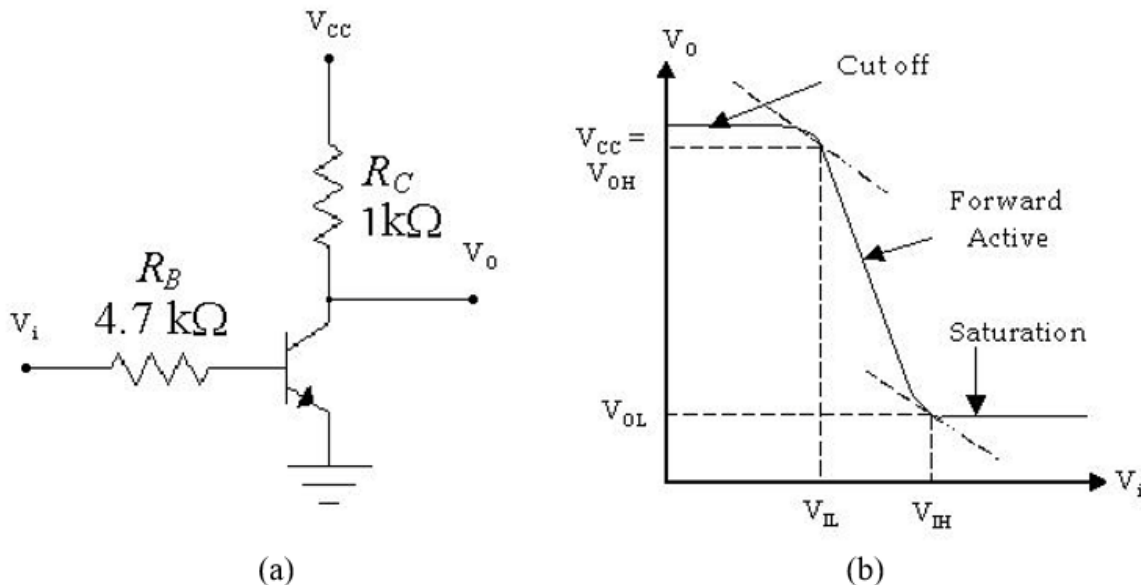


Figure 1 : The BJT inverter and its transfer characteristics

The propagation delay  $t_p$  is the difference between the times for which the input and output voltages are at their 50% values. The propagation delay time  $t_{pLH}$  is the delay time when the output changes from LOW to HIGH. Similarly, the propagation delay time  $t_{pHL}$  is the time when

the output changes from HIGH to LOW. The smaller the delay time, the faster is the operation of the logic gate.

### PROCEDURE:

1. Construct the circuit as show in Figure 2, using BJT, 100 k $\Omega$  potentiometer, and two resistors. Adjust the dc supply to 5 volts.

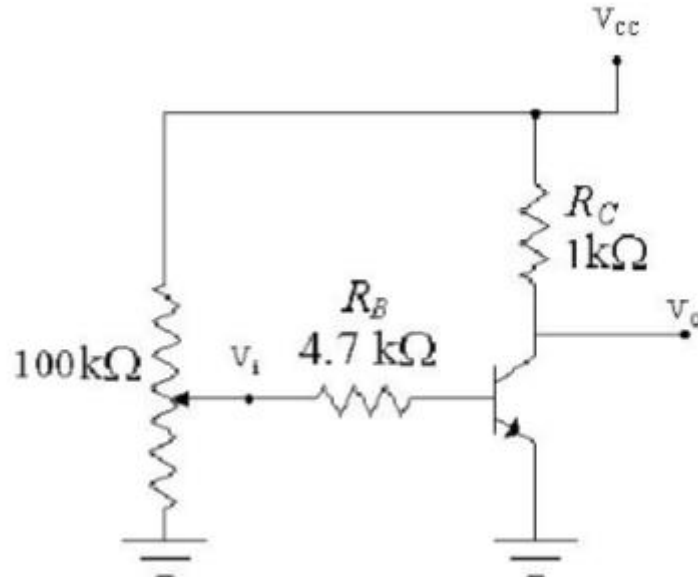


Figure 2 : Circuit Diagram .

2. Increase the input voltage  $V_i$  from 0 to 5 volts in small steps and for each step record the output voltage  $V_o$  in Table I for the following values of  $V_i$ .

3. Using the results obtained in step 2 above, plot the voltage transfer characteristics ( $V_o$  versus  $V_i$ ). From these characteristics determine the noise margins by completing the entries in Table II. Also, identify the uncertainty region on the plot.

4. Remove the potentiometer from the circuit of Figure 2, and connect a function generator at the input of the inverter ( $V_i$ ). Adjust the function generator to get a triangular waveform of 6V (Peak-to-Peak) at 60 HZ. Observer  $V_i$  on channel 1 and  $V_o$  on channel 2 of the oscilloscope. Plot these waveforms on a graph paper with proper scales.

5. Set the oscilloscope to X-Y mode and plot the transfer characteristics as displayed on the oscilloscope.

6. Adjust the function generator to get a square waveform of 6V (Peak to Peak) at 20 KHZ. Plot the displayed input and output waveforms on the graph paper.

7. Using the waveforms obtained in step 6, determine the propagation delay times,  $t_{pHL}$  and  $t_{pLH}$



Table I: Output voltage versus the input voltage.

$V_i$ (V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
$V_o$ (V)									
$V_i$ (V)	1.0	1.2	1.4	1.6	1.8	2.0	3.0	4.0	5.0
$V_o$ (V)									

Table II: Determination of the noise margins.

$V_{OH}$ (V)	$V_{IH}$ (V)	$NM_H$ (V)	$V_{IL}$ (V)	$V_{OL}$ (V)	$NM_L$ (V)

### DISCUSSION:

1. Give your detailed comments about the results obtained in this experiment.
2. Are the noise margins of this inverter appropriate for general-purpose applications?
3. Which delay time is greater than the other, and why?
4. How you improve the switching speed of this inverter? Explain in detail.

### PRE-LAB:

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.1
2. Simulate circuit of Fig. 1, using PSPICE.

### EXPERIMENT # 3: DIODE-TRANSISTOR LOGIC (DTL)

#### OBJECTIVES:

To understand the function of a simplified DTL NAND gate.

**EQUIPMENTS:** Power supply, digital multimeter, resistors, BJT, diodes.

#### BACKGROUND:

The simplified DTL NAND gate constructed in this experiment is basically developed from the diode logic AND gate and the BJT inverter.

#### PROCEDURE:

1. Construct the circuit as shown in Figure 1.

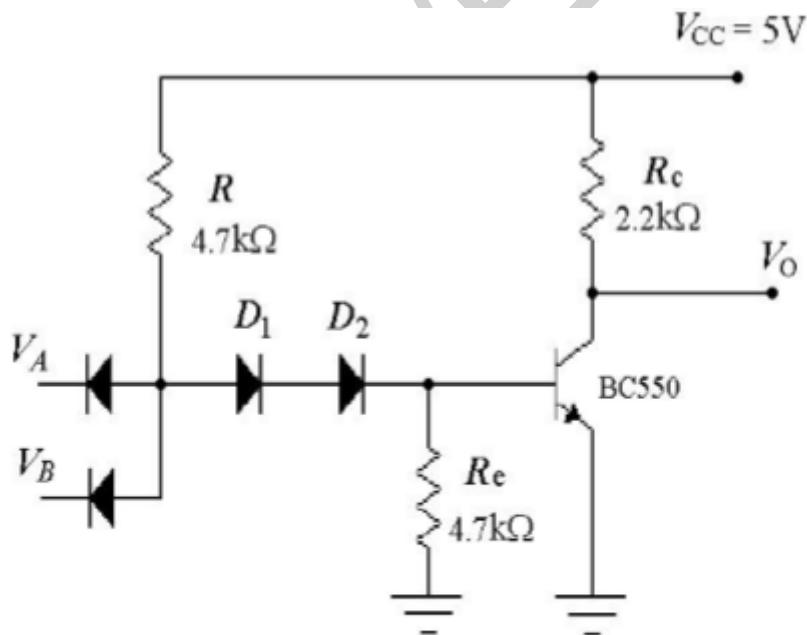


Figure 1 : Simplified DTL NAND gate.

2. Apply different input voltages as given in Table I and measure the output voltage  $V_O$ .

3. Replace diode  $D_2$  with a short-circuit and once again measure the output voltage for each combination of the input voltages as given in Table I.

Table I: DTL NAND gate results

$V_A$ (Volts)	$V_B$ (Volts)	$V_O$ (Volts) (with $D_2$ )	$V_O$ (Volts) (without $D_2$ )
0	0		
0	5		
5	0		
5	5		

**DISCUSSION:**

1. Explain the operation of the circuit shown in Figure 1.
2. When do you really need to put diode  $D_2$
3. From your results obtained in Table I, verify that the circuit functions as a NAND gate.

**PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.1
2. Simulate circuit of Fig. 1, using PSPICE.

## EXPERIMENT # 4: MODIFIED DTL NAND GATES

### OBJECTIVES:

- I. To investigate the operation of the circuit and to calculate its noise margins.
- II. Determine the fanout of the circuit and compare it with the theoretical values.

**EQUIPMENT:** Power supply digital multimeter, potentiometer (100 k $\Omega$ ), transistors, diodes and resistors.

### BACKGROUND:

In Experiment 3, a simple DTL NAND gate was studied. That circuit is modified by replacing the diode D1 with a transistor T1 so that there is an increase in the base current of the output transistor without a corresponding increase in the current load imposed by each additional gate. Thus, the fanout of the gate is considerably increased. This circuit is shown in Figure 1.

### PROCEDURES:

1. Construct the circuit as shown in Figure 1. Adjust the dc supply to 5 volts.

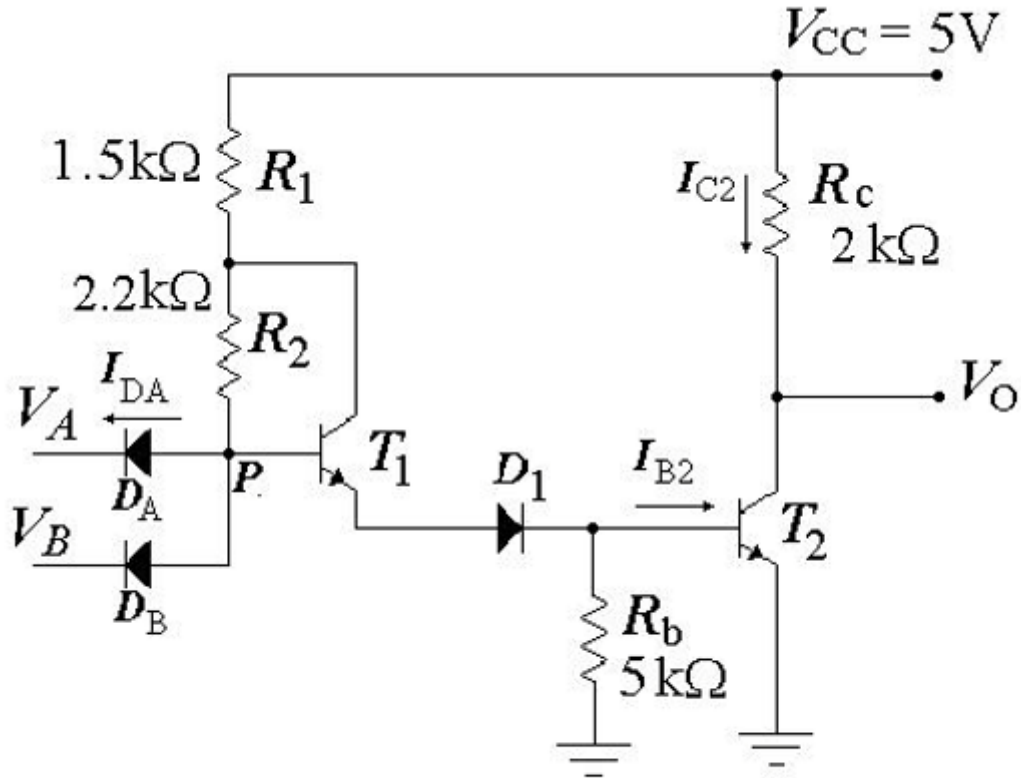


Figure 1 : Modified DTL NAND gate .

2. Measure the output voltage for each set of input voltages as given in Table I.
3. Set  $V_B$  to 5 volts (Logic '1').

Table I: Input/Output Relationship

$V_A$ (Volts)	$V_B$ (Volts)	$V_O$ (Volts)
0	0	
0	5	
5	0	
5	5	

4. Connect the 100 kΩ potentiometer to input  $V_A$  as shown in the Figure 2. Increase the input voltage  $V_A$  from 0 to 5 volts in small steps and for each step record the output voltage  $V_O$  in Table II. Note: You may need to record some additional readings around the cut-in voltage.

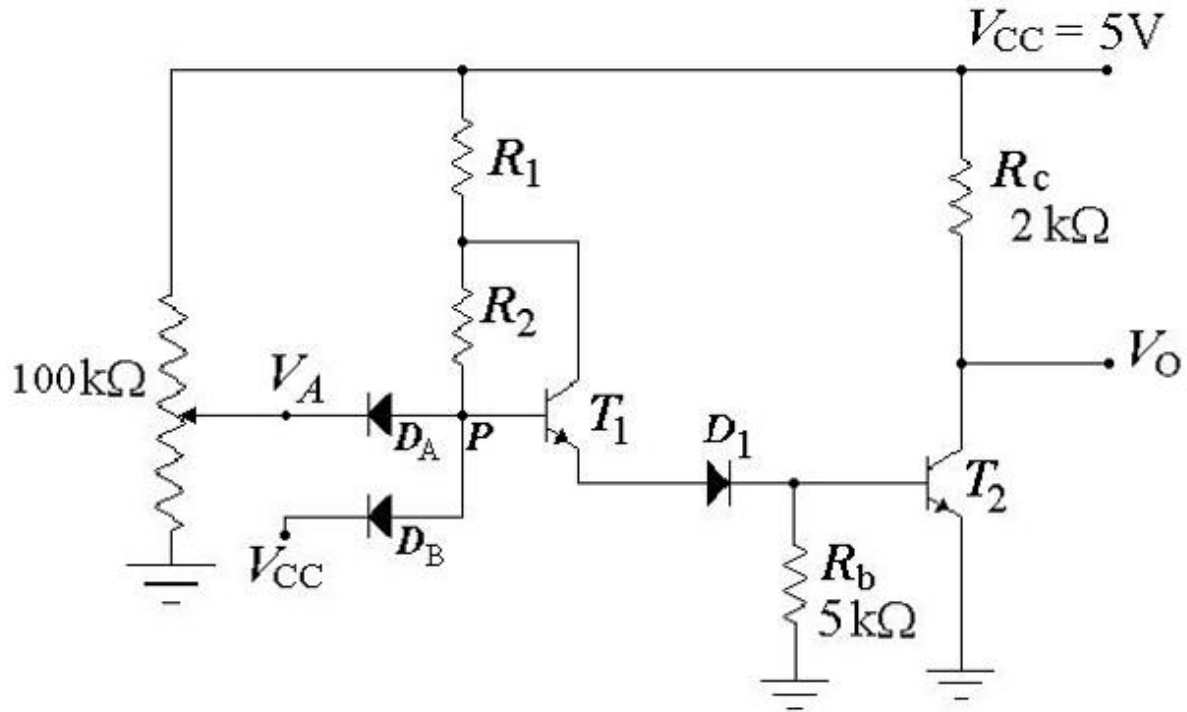


Figure 2 : Circuit for input  $V_A$  through potentiometer.

Table II: Output voltage  $V_O$  versus input voltage  $V_A$  for  $V_B$  set to logic '1'

$V_A$ (V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
$V_O$ (V)										
$V_A$ (V)	1.2	1.4	1.6	1.8	2.0	2.2	2.6	3.0	4.0	5.0
$V_O$ (V)										

5. Using the results obtained in step 4 above, plot the voltage transfer characteristics ( $V_O$  versus  $V_A$ ). From these characteristics determine the noise margins by completing the entries in Table III.

Table III: Determination of the noise margins for the Modified DTL gate.

$V_{OH}$ (V)	$V_{IH}$ (V)	$NM_H$ (V)	$V_{IL}$ (V)	$V_{OL}$ (V)	$NM_L$ (V)

6. Remove the potentiometer from the circuit of figure 2. Connect  $V_A$  to ground logic '0' through an ammeter. Measure the current passing through diode  $D_A$ .

7. Disconnect the ammeter, and connect  $V_A$  to  $V_{CC}$  logic '1'. Measure the voltage at point P, shown in Figure 2.

8. Keeping  $V_A$  at logic level '1', measure voltages across resistors  $R_1$ ,  $R_2$ ,  $R_b$  and  $R_c$ .

9. Disconnect the circuit from the supply. Remove the resistor  $R_1$ ,  $R_2$ ,  $R_b$  and  $R_c$ . And measure their actual values.

## **DISCUSSION:**

1. Describe the effect of the value chosen for resistor  $R_b$ . How the circuit will perform if:
  - i)  $R_b$  is very large
  - ii)  $R_b$  is very small
2. Can  $R_1$  have a value higher than  $R_2$  ? Explain.
3. Why this circuit is better than the simplified DTL gate studied in experiment3.
4. Compare the measured value of  $I_{DA}$  in step 6 of the procedure with its theoretical value. Show all the steps.
5. Using the measured values of voltages across resistors  $R_1$ ,  $R_2$ ,  $R_b$  and  $R_c$ , and their resistances, calculate the currents flowing through these resistors when  $V_A$  and  $V_B$  were both at logic '1'. Show that  $T_1$  is in active mode, while transistor  $T_2$  is in saturation. (You may determine the approximate value of  $hFE (= \beta)$  of transistor  $T_1$  from measured and calculated data available to you.)
6. Using the currents as determined in step 5 above and the value of  $I_{DA}$  measured in step 6 of the procedure, determine the fanout of this gate.

## **PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.1
2. Simulate circuit of Fig. 1, using PSPICE.

## EXPERIMENT # 5: TRANSISTOR-TRANSISTOR LOGIC (TTL)

### OBJECTIVE:

To study a TTL NAND gate by using a circuit made from discrete components as well as by using an integrated circuit TTL NAND gate.

**EQUIPMENT:** Power supply, oscilloscope, digital multimeter, potentiometer (100 k $\Omega$ ), transistors, diodes and resistors.

### BACKGROUND:

TTL gates are among the most popular logic families, and a variety of gates are available in this family. The major limitation of the TTL gates are among the most popular logic families, and a variety DTL NAND gate studied in Experiment 3 is its speed of operation, which is overcome in the TTL NAND gate studied in this experiment. The input transistor for a TTL NAND gate is a multi-emitter transistor. For this experiment, a "multi-emitter" transistor can be made by using two transistors connected as shown in figure 1.

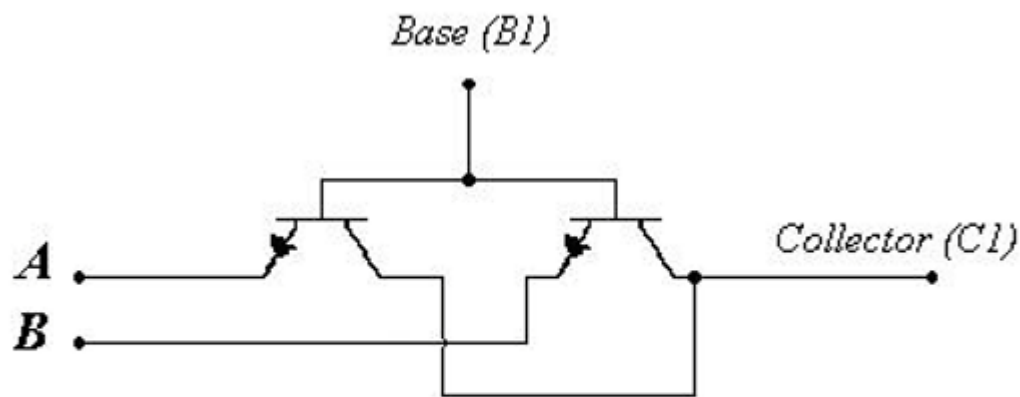


Figure 1 : Forming a " multi-emitter " transistor.

### PROCEDURE:

1. Construct the circuit as shown in Figure 2. Adjust the dc supply to 5 volts.
2. Connect a load resistor  $R_L$  of 1 k $\Omega$  at the output terminals. For different values of input voltages, measure the voltage  $V_{CE}$  for each transistor and record it in Table I. Note that the output voltage  $V_O = V_{CE}$
3. Remove the load resistor.



4. With  $V_A = 0$  V, set  $V_B$  to 5 volts (logic '1'). Measure  $V_{Rb}$

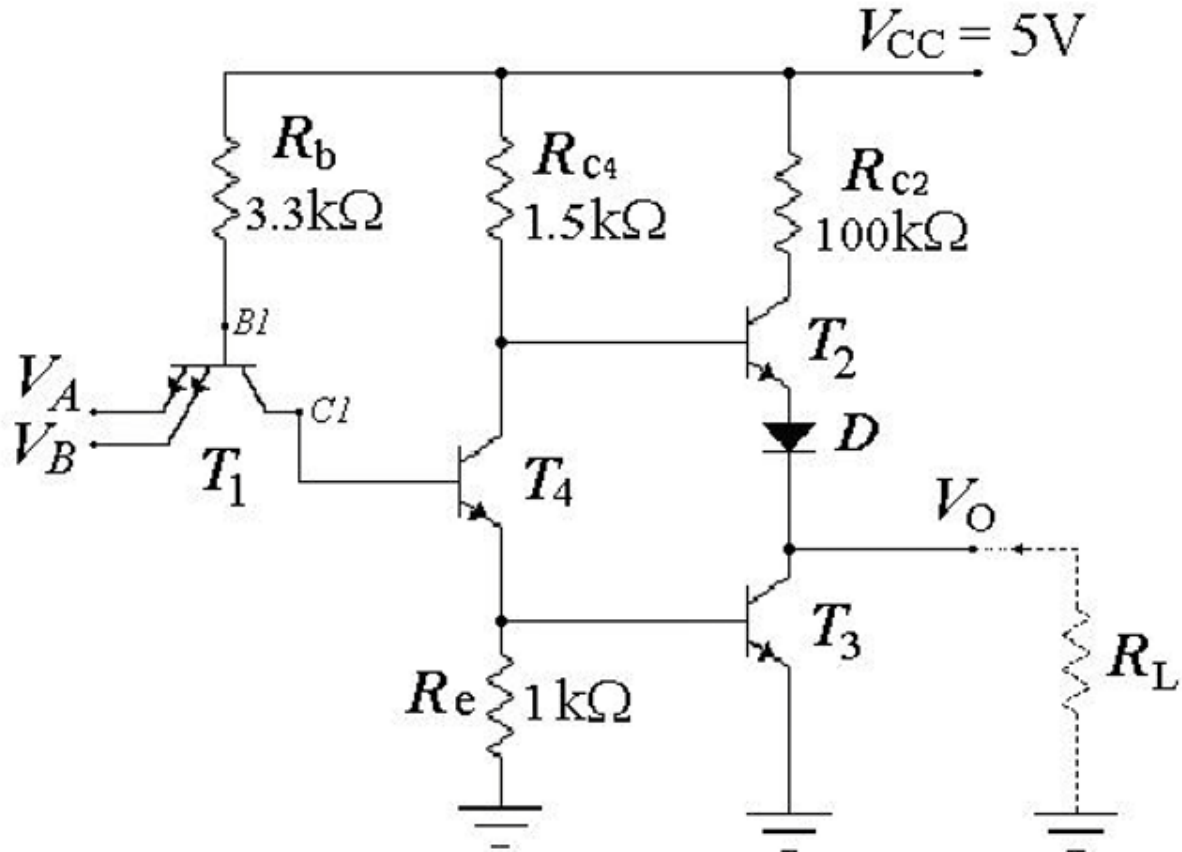


Figure 2 : TTL NAND gate using discrete components

Table I: Measurements of transistors collector-emitter voltages (all in volt).

$V_A$	$V_B$	$V_{CE1}$	$V_{CE2}$	$V_{CE3}$	$V_{CE4}$	$V_O$
0	0					
0	5					
5	0					
5	5					

5. Set  $V_A = V_B = 5$  Volts. Measure  $V_{Rb}$ ,  $V_{RC4}$  and  $V_{Re}$ .

6. Keep  $V_B$  as 5 V (logic '1'). Connect the 100 kΩ potentiometer to provide a variable input  $V_A$ . Increase the input voltage  $V_A$  from 0 to 5 volts in small steps and for each step record the output voltage  $V_O$  in Table II. Note: You may need to record additional readings around the cut-in voltage.

Table II: Output voltage  $V_O$  versus the input voltage  $V_A$ , for  $V_B$  set to logic '1'

$V_A$ (V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
$V_O$ (V)									
$V_A$ (V)	1.0	1.2	1.4	1.6	1.8	2.0	3.0	4.0	5.0
$V_O$ (V)									

7- Using the results obtained in step 6 above, plot the voltage transfer characteristics ( $V_O$  versus  $V_A$ ). From these characteristics determine the noise margins by completing the entries in Table III.

Table III: Determination of the noise margins for the TTL NAND gate.

$V_{OH}$ (V)	$V_{IH}$ (V)	$NM_H$ (V)	$V_{IL}$ (V)	$V_{OL}$ (V)	$NM_L$ (V)

8. Remove the potentiometer. Keeping input  $V_B$  as HIGH, apply a square wave of 10Vp-p (100HZ) at input  $V_A$ . Observe the output voltage  $V_O$  on the oscilloscope and plot both input and output voltages on a graph paper. Repeat this with capacitive loads of  $0.47\mu\text{F}$  and  $4.7\mu\text{F}$ .

9. Disconnect the circuit and measure the resistance of the entire resistor. Record their values.

### DISCUSSION:

1. On the basis of measured voltages in Table I, determine the mode of operation of each transistor for various combinations of input voltages.
2. Using the voltages measured in step 4 and step 5, and the measured values of resistors, calculate various currents to determine the fanout of the gate. Mention any assumptions you need to make.
3. Comment on the results obtained in step 8 above.
4. How the output waveforms will look different from those obtained in step 8, if the active pull-up in the circuit was replaced by a passive pull-resistor. Explain.

### PRE-LAB:

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.2
2. Simulate circuit of Fig. 2, using PSPICE.

## EXPERIMENT # 6: TTL DESIGN PROJECT

### OBJECTIVES:

To design and test a TTL NOR gate by using a circuit made from discrete components.

**EQUIPMENTS:** Power supply, function generator, oscilloscope, digital multimeter, diodes, transistors, potentiometer (100 k $\Omega$ ), and resistors.

### PROCEDURE:

1. Construct the circuit as shown in Figure 1. Adjust the dc supply to 5 volts.

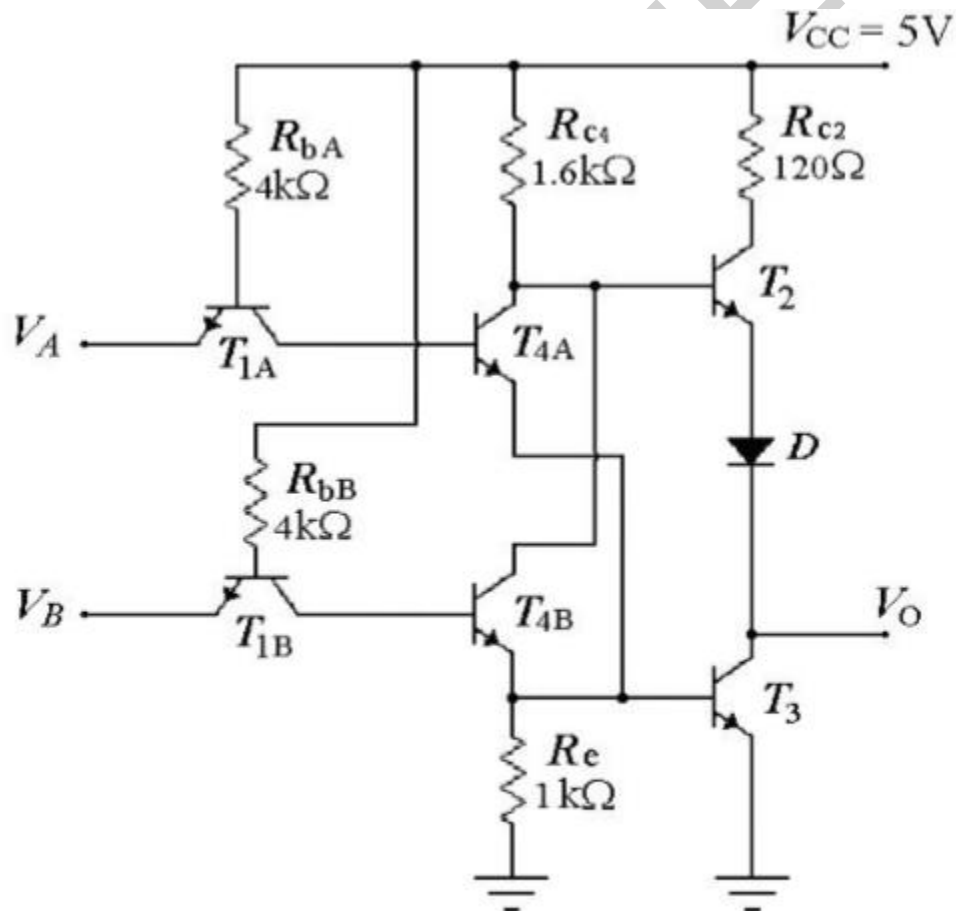


Figure 1 : TTL NOR .

2. For different values of input voltages, measure the output voltage  $V_O$  for circuit and record it in Table I.

3. Set  $V_B = 0$  (logic '0'). Connect the 100 k $\Omega$  potentiometer  $V_A$  from 0 to 5 volts in small steps & for each step record the output voltage  $V_O$  in Table II.

Table I: Input/Output voltages.

$V_A$ (Volts)	$V_B$ (Volts)	$V_O$ (Volts)
0	0	
0	5	
5	0	
5	5	

Table II: Output voltage  $V_O$  versus the input voltage  $V_A$  for  $V_B$  set to logic '0'

$V_A$ (V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
$V_O$ (V)									
$V_A$ (V)	1.0	1.2	1.4	1.6	1.8	2.0	3.0	4.0	5.0
$V_O$ (V)									

4. Using results obtained in step 3 above, plot the voltage transfer characteristics ( $V_O$  versus  $V_A$ ). Determine the noise margins by completing Table III.

Table III: Determination of the noise margins for the TTL NOR gate.

$V_{OH}$ (V)	$V_{IH}$ (V)	$NM_H$ (V)	$V_{IL}$ (V)	$V_{OL}$ (V)	$NM_L$ (V)

5. Remove the potentiometer and use two-function generators, one for  $V_A$  & other one for  $V_B$ . Apply a square-wave of 10 Vp-p (1kHz) at  $V_A$  and a square-wave of 10 Vp-p (2kHz) at input  $V_B$ .

6. Observe the output  $V_O$  and plot both inputs voltages & the output voltage on a graph paper.

### DISCUSSION:

1. Theoretically, calculate the output voltage for different states of inputs and plot the voltage transfer characteristics. Compare it with the experimental results.

2. Repeat steps 5 & 6, using SPICE analysis (such as Electronic-Work-Bench 5 or Orcad 9).

3. Plot the voltage-transfer characteristics using the SPICE analysis.

**PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.1
2. Simulate circuit of Fig. 1, using PSPICE.

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## EXPERIMENT # 7: RESISTOR-LOADED NMOS INVERTER

### OBJECTIVES:

- I. To determine the values of parameters 'k' and 'V<sub>T</sub>' of the given NMOS and plot its output characteristics.
- II. To plot the voltage transfer characteristics of the NMOS inverter with resistive load and determine the noise margins.

**EQUIPMENT:** Power supply, digital multimeter, potentiometer, N-MOSFET and resistors.

### BACKGROUND:

The current  $I_D$  for NMOS is given as,

1. Ohmic (Linear) Region: ( $V_{DS} \leq V_{GS} - V_T$ )

$$I_D = k [2 (V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

2. Saturation Region: ( $V_{DS} \geq V_{GS} - V_T$ )

$$I_D = k [(V_{GS} - V_T)^2]$$

Once the values of parameters k and  $V_T$  are known, the output characteristics of NMOS can be plotted. (You may use a computer program for plotting)

### PROCEDURE:

1. Connect the circuit as shown in the Figure 1. Note that for this connections  $V_{DS} = V_{GS}$  and the NMOS will be in the saturation mode.
2. For different values of the variable resistor  $R_V$  measure  $V_{DS}$  and  $I_D$ . Record these values in Table I.

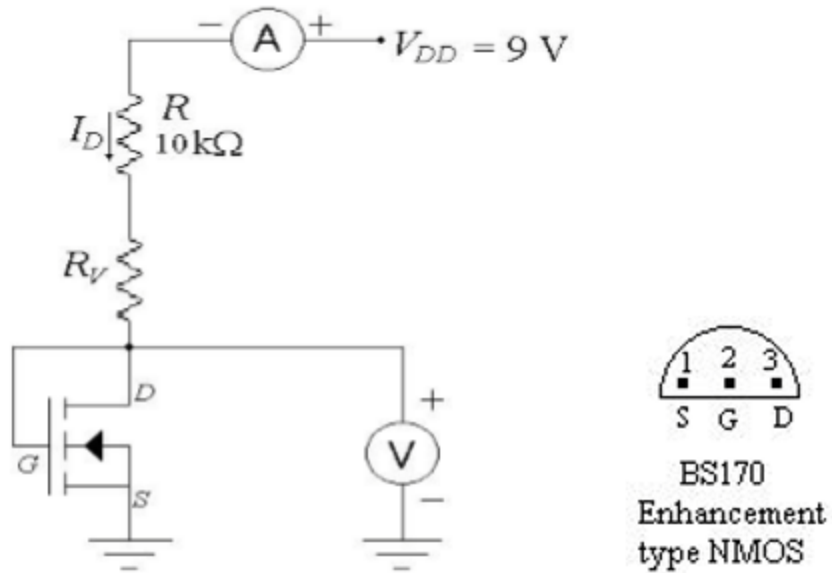


Figure 1 : Circuit for determining NMOS parameter.

Table I: Measured values of drain current and drain-to-source voltage.

$I_D$ ( $\mu\text{A}$ )										
$V_{DS}$ (V)										
$I_D$ ( $\mu\text{A}$ )										
$V_{DS}$ (V)										

- Plot  $\sqrt{I_D}$  versus  $V_{GS}$  ( $=V_{DS}$ ).
- Find  $V_T$  from the intersection of the resulting straight line and  $V_{GS}$  axis. The equation of this straight line is,
 
$$\sqrt{I_D} = \sqrt{k} [(V_{GS} - V_T)]$$
- From the slope of the straight line obtained in step 3, determine value of  $k$ .
- Plot the output characteristics  $I_D$  versus  $V_{DS}$  using the data in Table I. Identify the ohmic and saturation region.
- Connect the circuit as shown in Figure 2. Use  $R_D = 10 \text{ k}\Omega$ .

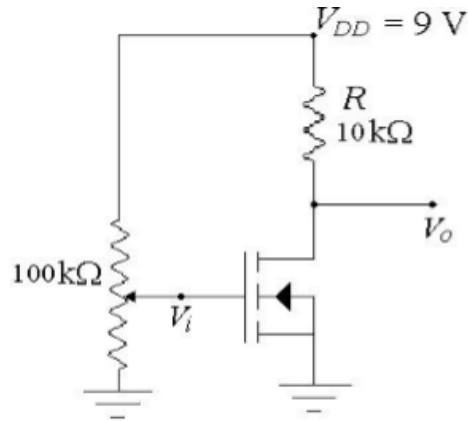


Figure 2 : NMOS inverter with resistive load (Determination of Transfer Characteristics )

8. For different values of  $V_i$  measure the output voltage  $V_o$ . Record your data in Table II. You should take more readings when  $V_T - 0.5 \leq V_i \leq V_T + 1$ .
9. Using the data in Table II, plot the transfer characteristics. Compare the noise margins.
10. Change  $R_D$  to  $47 \text{ k}\Omega$  and repeat steps 8 & 9. Record your data in Table III.

Table II: Data for voltage transfer characteristics ( $R_D = 10 \text{ k}\Omega$ )

$V_i$ (V)										
$V_o$ (V)										
$V_i$ (V)										
$V_o$ (V)										

Table III: Data for voltage transfer characteristics ( $R_D = 47 \text{ k}\Omega$ )

$V_i$ (V)										
$V_o$ (V)										
$V_i$ (V)										
$V_o$ (V)										

### DISCUSSION:

1. Prove that the NMOS, as shown in Figure 1, is in saturation mode.
2. Comment on the effect of different values of  $R_D$ .
3. Mention one advantage and one disadvantage of using higher value of  $R_D$  in the inverter circuit.
4. Why resistors are preferably replaced by MOSFETs in integrated circuits?
5. What have you learned after this experiment?



**PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.2.
2. Simulate circuit of Fig. 2, using PSPICE.

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## EXPERIMENT # 8 : CMOS INVERTER

### OBJECTIVES:

To plot the voltage transfer characteristics of the CMOS inverter and determine the noise margins. Calculating the power dissipation.

**EQUIPMENTS:** Power supply, digital multimeter, potentiometer, and CMOS.

### BACKGROUND:

CMOS is currently the most popular digital circuit technology. CMOS logic circuits are available as standard SSI and MSI packages for use in conventional digital system design. CMOS is also used in general-purpose VLSI circuits such as memory and microprocessors.

The CMOS Inverter is shown in figure 1. It consists of an N-channel MOSFET and a Pchannel MOSFET. The input is applied to the two gates. The substrate of each transistor is connected to the source, and therefore no body effect for both transistors. When  $V_i$  is high,  $Q_N$  is ON and  $Q_P$  is OFF. The output is low and  $V_{OL} \approx 0$  (typically less than 10mV). If  $V_i$  is low,  $Q_N$  is OFF and  $Q_P$  is ON. The output is high with  $V_{OH} \approx V_{DD}$  (typically less than 10mV below  $V_{DD}$ ). Since the inverter current as zero in each case; the static power dissipation is zero (typically a fraction of  $\mu w$ ).

The voltage transfer characteristic has a linear part is an infinite slop. This part is obtained when both transistors are saturated. Therefore, this inverter approximates the ideal inverter.

### PROCEDURE:

1. Connect the circuit shown in Figure 1. Set the supply to 5V.
2. For different values of  $V_i$  in range of 0 to 5V, measure the output voltage  $V_o$  and current from supply  $I_{DD}$ . Record your data in Table I. Take more readings around the point of maximum conducting for  $I_{DD}$ .
3. Plot the voltage-transfer characteristics, and determine the values of noise margins.
4. Plot the power dissipation against the input voltage. (Hint: use the measured supply current  $I_{DD}$  times the supply voltage  $V_{DD}$ ).

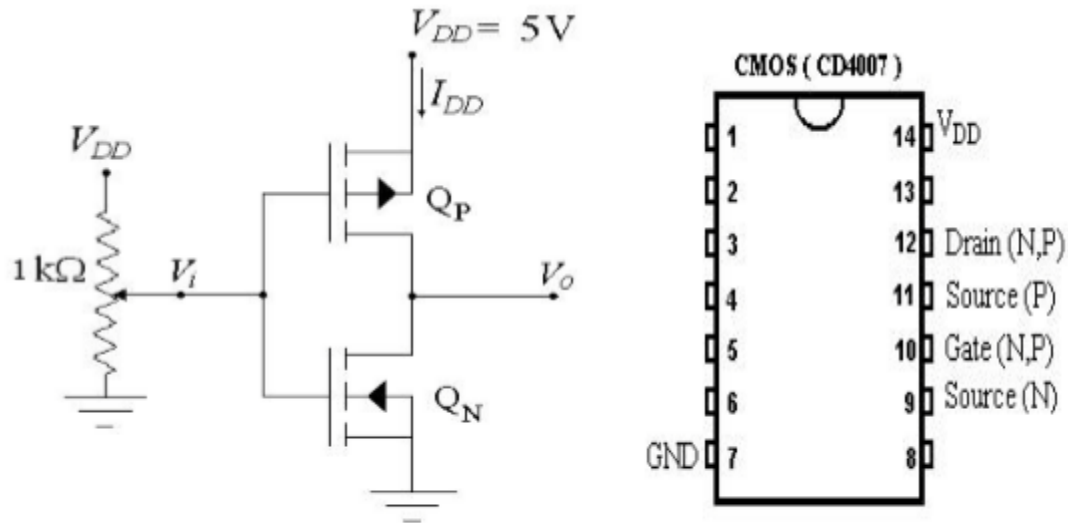


Figure 1: CMOS inverter and IC Chip (CD4007).

Table I: Input / Output voltages and supply current measured for the CMOS inverter.

$V_i$ (V)	0	0.2	0.5	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.1	2.2	2.3	2.4	2.5
$V_o$ (V)															
$I_{DD}$ (mA)															
$V_i$ (V)	2.6	2.7	2.8	2.9	3.0	3.1	3.2	3.4	3.6	3.8	4.0	4.2	4.5	4.8	5.0
$V_o$ (V)															
$I_{DD}$ (mA)															

### DISCUSSION:

1. Compare the VTC of this inverter versus that of the NMOS inverters with saturated enhancement load.
- 2..At which input and output voltage the power dissipation is maximum?
3. From your results, do you think that this CMOS Inverter is a Symmetric CMOS Inverter or not? Prove it.
4. On the VTC plot and the power dissipation plot, mention the mode of operation of each transistor ( $Q_P$  and  $Q_N$ ).

### PRE-LAB:

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.1.
2. Simulate circuit of Fig. 1, using PSPICE.

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## EXPERIMENT # 9: EMITTER-COUPLED LOGIC (ECL)

### OBJECTIVE:

To demonstrate the operation of a simplified version of the ECL gate made by using discrete components.

**EQUIPMENTS:** Power supply, digital multimeter, potentiometer (100 k $\Omega$ ), diodes, transistors and resistors.

### BACKGROUND:

The first part of this experiment deals with the reference voltage used in the ECL circuit. The experimentally measured value will be compared with the theoretically calculated value. In the second part, a two-input ECL gate will be made excluding the emitter-follower output stages.

### PROCEDURE:

1. Construct the circuit as shown in figure 1. Adjust the potentiometer to get -5V at VEE.
2. Measure the reference voltage  $V_R$ .
3. Construct the simplified ECL gate excluding the output stages as shown in Figure 2.
4. Let  $V(1) = -0.75$  V and  $V(0) = -1.75$  V. For different combinations of voltages, measure the two output voltages and record their values in Table I. Also, measure the voltage at point E in the circuit shown in Figure 2.

Table I: Measurements of voltages for the ECL gate

$V_A$ (Volts)	$V_B$ (Volts)	$V_{O1}$ (Volts)	$V_{O2}$ (Volts)	$V_E$ (Volts)
- 1.75	- 1.75			
- 1.75	- 0.75			
- 0.75	- 1.75			
- 0.75	- 0.75			

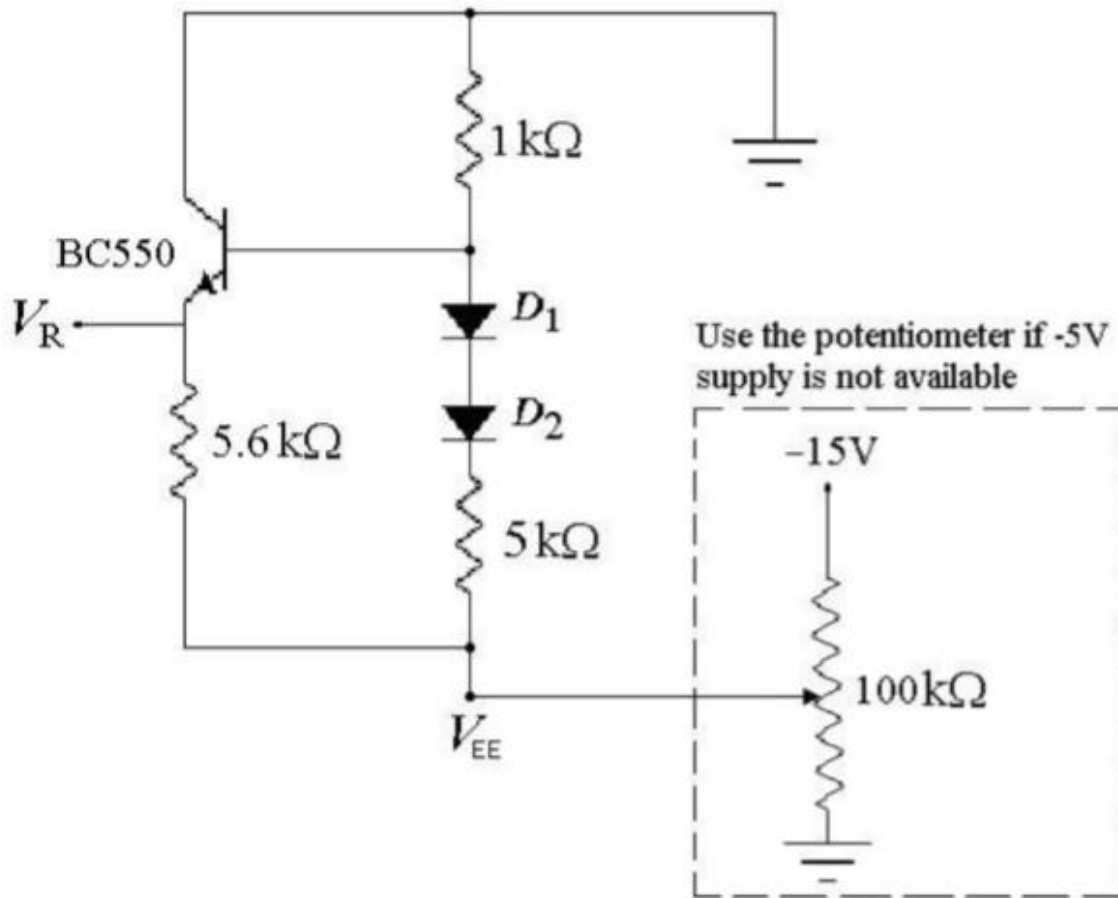


Figure 1 : Circuit for obtaining reference voltage.

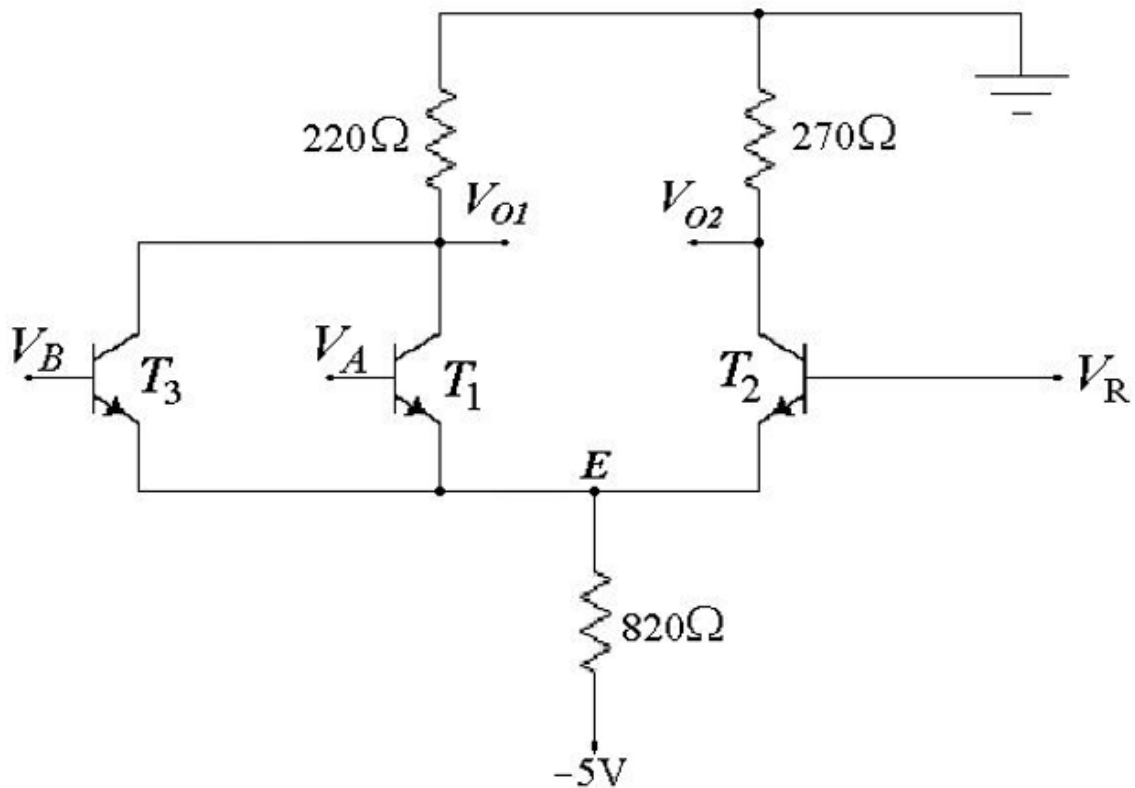


Figure 2 : Simplified ECL gate.

Table II : Output voltage  $V_{O2}$  versus the input voltage  $V_A$  for  $V_B$  set to logic '0'

$V_A$ (V)	0.0	-0.2	-0.3	-0.4	-0.5	-0.6	-0.7	-0.8	-0.9
$V_{O2}$ (V)									
$V_A$ (V)	-1.0	-1.1	-1.2	-1.3	-1.4	-1.5	-1.6	-1.8	-2.0
$V_{O2}$ (V)									

6. Using the results obtained in step 4 above, plot the voltage transfer characteristics ( $V_{O2}$  versus  $V_A$ ). From these characteristics determine the noise margins by completing the entries in Table III.

Table III: Determination of the noise margins for the ECL gate.

$V_{OH}$ (V)	$V_{IH}$ (V)	$NM_H$ (V)	$V_{IL}$ (V)	$V_{OL}$ (V)	$NM_L$ (V)

7. Disconnect the circuit and measure the resistances of all the resistors used in the experiment. Record their values.

## **DISCUSSION:**

1. Compare the experimentally obtained value of reference voltage  $V_R$  with the theoretically calculated value. Explain the difference between the two values.
2. On the basis of measured voltages in Table I, identify which output is for OR operation and which output is for NOR operation .
3. Using the measured voltages in Table I, determine the mode of operation of each transistor for various combinations of input voltages. Compare your results with theoretically expected modes of operation for these transistors.
4. Why the two levels of output voltage are not the same as the logic '0' and logic '1' voltages used in the experiment. Explain

## **PRE-LAB:**

The following pre-lab must be completed and submitted before the start of this experiment. The pre-lab shall be graded and is part of your lab grades.

Solve the following exercises on separate sheets of paper and submit your solution before the start of the lab experiment.

1. Analyze the circuit of Fig.2
2. Simulate circuit of Fig. 2, using PSPICE.